Mrigank Sharma
mriganks@ece.ubc.ca
778-865-2284

**Academic Positions Held**

- Research Assistant with Dr. Edmond Cretu (fall 2006-2008)
- Teaching Assistant for EECE 353 (fall 2007)
- Associate Vice President Administration at Graduate Student Society (April 2007-2008)
- Undergraduate Research trainee at WAran Research FoundaTion(WARFT)(August 2004-2006)

**Academic Scores**

- Master's of Applied Science (ECE)- The University of British Columbia (2006-2008) with **83%**
  **Thesis :** "The Design and Modeling of Advanced Gyroscopes**" (to be marked)**
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  Bachelor's of Engineering (ECE)-Anna University (2002-2006) with **80%**
  **Project:** Low Power FPGA Architecture And Mapping Techniques. (**Best Project with 198/200 in University exam)**

**Research Interests**

- MEMS, BIOMEMS, NANO TECHNOLOGY, CAD VLSI, MIXED SIGNAL, LOW POWER FPGA ARCHITECTURES.

**Research Experience(2006-2007)**

**Coventorware-** For Modeling Resonant Structures, Did system level simulations for o-MEMS project which was used in Yiyi Zheng's thesis (http://www.mina.ubc.ca/project_o-mems-accelerometer-gyroscope)

**Matlab/Mathematica-** Used extensively for Noise analysis Modeling of Damping for a paper.

**Probe Station /Clean Room** – Worked with probe station to actuate the resonator. Helped a colleague with his clean room visits.

**SPICE**- Used SPICE extensively for designing the read out circuitry.

**FEA (Coventor)-** For Damping Analysis.

**VHDL Coding** – TA of a course which has lab with VHDL coding and FPGAs.

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**Research Experience (2004-2006)**

- Had a 2-year research training program at **WA**ran **R**esearch **F**ounda**T**ion (WARFT), Marconi (Mixed Signal group),Viswakarma (High Performance Group). www.warftindia.org <http://www.warftindia.org/> .

**Research Publications**
( http://www.warftindia.org/generic.php?cat=paps <http://www.warftindia.org/generic.php?cat=paps> )

- "Digital Model For Interconnect Analysis", 23 rd IEEE CAS NORCHIP Conference, Finland.
- "Analysis Of Cross Talk Masking Of Electromigration And On Chip Tracking Of Interconnect Agieng".14 th IEEE NORTH ATLANTIC TEST WORKSHOP, Vermont USA.

**Publication Under Review(Journal Paper )**

"A Massively Parallel FPGA Architecture for High Performance Computing", IEEE Transaction on VLSI.

**Tool Developed By Me**
( http://www.warftindia.org/generic.php?cat=tool <http://www.warftindia.org/generic.php?cat=tool> )

Digital Interconnect Model For Clock Integrity Analysis.

**White Paper At WARFT**

"Interconnect Length Prediction For MIP S.C.O.C ": Part I Memory In Processor Super Computer on a Chip (MIP S.C.O.C) White paper.

**Invited Lecture**

(http://www.warftindia.org/generic.php?cat=dhiy)

-Power and Signal Integrity Issues

-Interconnect Modeling

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**Extra curriculum Activities**

- Represented TAMIL NADU state in ALL INDIA NATIONAL ROLLER SKATING competition in Dec 99 held at Pune.
- Represented Chennai Zone(Tamil Nadu, Kerela, Pondicherry) in ALL INDIA K.V. SPORTS meet in Tennis held at Delhi in 2000.
- Scholarship Holder For Tennis given by Kendriya Vidhalaya Sangathan.
- Math Club President in VanaVani Higher secondary school (IIT MADRAS).year(2001-2002).
- Winner of Tennis Zonal in ANNA UNIVERSITY 2003,2004.
- Runners- up in TIES(Tamil Nadu Inter Engineering Sports meet) among 232 colleges in 2004.
- Scholarship winner (Travel) given by Hipc (International conference on High Performance Computing) Dec 2005 Goa.
- Have about twenty medals of State level in Tennis and Skating.

**REFERENCES**

1)Dr Edmond Cretu Phone: 1-604-827-4115 (direct line), email edmondc@ece.ubc.ca

2) Professor N.Venkateswaran Phone: (91) (44) 24899766, email waran@warftindia.org